

**What is claimed is:**

- Sub 1/2
- 1 1. An integrated circuit structure comprising:
    - 2 a semiconductor layer having a major surface formed along a plane;
    - 3 first and second spaced-apart doped regions formed in the surface;
    - 4 a third doped region over the first region of different conductivity type than the
    - 5 first region; and
    - 6 a conductive layer formed between the first and second regions and above the
    - 7 plane, providing electrical connection between the doped regions.
  - 1 2. The structure of claim 1 wherein the first doped region is a first
  - 2 source/drain region of a MOSFET and the third region is a channel region of the
  - 3 MOSFET.
  - 1 3. The structure of claim 2 wherein the second region is a portion of a
  - 2 transistor.
  - 1 4. The structure of claim 2 wherein the second region is a second
  - 2 source/drain region associated with a second MOSFET, said structure further comprising
  - 3 a channel region of the second MOSFET aligned with the second source/drain region.
  - 1 5. The structure of claim 1 further including:
    - 2 a fourth doped region over the second region of different conductivity type than
    - 3 the second region;
    - 4 a fifth doped region over the fourth doped region of the same conductivity type as
    - 5 the second region;
    - 6 a sixth doped region over the third doped region of the same conductivity type as
    - 7 the first region, said first, second, third, fourth, fifth and sixth regions and conductive
    - 8 layer configured as two interconnected transistors.
  - 1 6. The structure of claim 5 wherein the two transistors are of complementary
  - 2 conductivity type.
  - 1 7. The structure of claim 5 wherein one of the transistors is a MOSFET.
  - 1 8. The structure of claim 5 wherein the transistors are configured to form an
  - 2 inverter circuit.

Sub 2  
1 9. The structure of claim 1 wherein the conductive layer comprises one or  
2 more materials taken from the group comprising tungsten silicide, tungsten nitride,  
3 titanium silicide, titanium nitride and cobalt silicide.

Sub a3  
1 10. The structure of claim 1 wherein the diffusion regions are configured to  
2 form an inverter circuit.

1 11. The structure of claim 1 wherein the first and second doped regions are  
2 first and second source/drain regions and the third region is a channel region, said  
3 structure further comprising:  
4 a second channel region formed over the second source/drain region;  
5 third and fourth spaced-apart source/drain regions each vertically aligned with one  
6 of the channel regions and one of the first and second source/drain regions; and  
7 a conductive element connected to simultaneously control operation of both  
8 transistors.

1 12. The structure of claim 11 wherein the conductive element comprises  
2 polysilicon and the transistors each include a gate contact region adjacent the channel  
3 region and connected to the conductive element, said transistors configured to form an  
4 inverter circuit function.

1 13. The structure of claim 1 wherein the conductive layer is a continuous film  
2 extending from the first region to the second region.

1 14. The structure of claim 1 wherein the conductive layer physically contacts  
2 the first region and the second region.

Sub B3  
1 15. A semiconductor device comprising:  
2 a first layer of semiconductor material;  
3 a first field effect transistor having a first source/drain region formed in the first  
4 layer, a channel region formed over the first layer and a second source/drain region  
5 formed over the channel region;  
6 a second field effect transistor having a first source/drain region formed in the  
7 first layer, a channel region formed over the first layer and a second source/drain region  
8 formed over the channel region; and

9 a conductive layer comprising a metal positioned between the first source/drain  
10 region of each transistor to conduct current from one first source/drain region to the other  
11 first source/drain region.

1 16. The device of claim 15 wherein the first and second transistors are  
2 connected to form a circuit.

1 17. The device of claim 15 comprising a plurality of additional field effect  
2 transistors each having a first source/drain region formed in the first layer, a channel  
3 region formed over the first layer and a second source/drain region formed over the  
4 channel region, the first, second and additional transistors configured into a circuit.

1 18. The device of claim 17 wherein four of the additional transistors are  
2 connected with the first and second transistors to form an SRAM circuit cell.

1 19. The device of claim 15 wherein the conductive layer comprises a metal  
2 silicide.

1 20. A method for fabricating a semiconductor device with a plurality of field  
2 effect transistors comprising:

3 forming a first device region, selected from the group consisting of a source  
4 region and a drain region of a field effect transistor, on a semiconductor layer;

5 forming a second device region, selected from the group consisting of a source  
6 region and a drain region of a field effect transistor, on the semiconductor layer;

7 forming a conductor layer comprising metal adjacent the first and second device  
8 regions to effect electrical connection between the first and second device regions;

9 forming a first field effect transistor gate region over the first device region and  
10 the conductor layer; and

11 forming a second field effect transistor gate region over the second device region  
12 and the conductor layer.

1 21. The method of claim 20 including the additional step of configuring the  
2 first and second device regions, the conductor layer and the first and second gate regions  
3 into a circuit comprising two MOSFET transistors.

1 22. The method of claim 20 further including the step of configuring the first  
2 and second device regions, the conductor layer and the first and second gate regions into

3 a circuit comprising two MOSFET transistors having drain regions connected to one  
4 another by the conductive layer.

1 23. A method for fabricating a semiconductor device with a plurality of  
2 transistors comprising:  
3 forming first and second spaced-apart diffusion regions on a semiconductor layer;  
4 positioning a conductor layer to effect electrical connection between the first and  
5 second diffusion regions;  
6 forming third and fourth semiconductor regions, each over a different one of the  
7 spaced-apart diffusion regions and over the semiconductor layer;  
8 forming fifth and sixth semiconductor regions each positioned over a different  
9 one of the third and fourth semiconductor regions such that the third and fifth regions are  
10 vertically aligned with one of the first and second regions and the fourth and sixth regions  
11 are vertically aligned with the other of the first and second regions, the resulting structure  
12 providing two transistors each having a region connected to the other transistor.

1 24. A method for fabricating an integrated circuit structure comprising:  
2 providing a semiconductor layer suitable for device formation thereon, said layer  
3 including a surface formed along a first plane;  
4 forming spaced-apart first and second trenches over the semiconductor layer;  
5 forming a conductor layer extending over the semiconductor surface between the  
6 first trench and the second trench;  
7 forming a plurality of dielectric layers over the metal conductor layer;  
8 forming a vertical transistor with first, second and third doped regions in the first  
9 trench with at least part of the first doped region formed in the semiconductor layer in  
10 electrical contact with the metal conductor layer.

1 25. The method of claim 24 wherein the step of forming the first and second  
2 trenches is performed after the dielectric layers are formed over the metal conductor  
3 layer.

1 26. The method of claim 24 further including the step of forming a second  
2 vertical transistor in the second trench with a first doped region of the second transistor  
3 formed in the semiconductor layer and making electrical contact with the metal conductor  
4 layer.

1           27.     The method of claim 24 wherein the step of forming each vertical  
2 transistor includes formation of source, channel and drain regions in a relatively vertical  
3 alignment with respect to the surface of the semiconductor layer.

1           28.     The method of claim 24 further including the step of forming a circuit  
2 including at least one connection to the transistor through the conductive layer.

1           29.     The method of claim 24 further including the steps of:  
2 forming a second vertical transistor in the second trench; and  
3 configuring the first and second transistors in a circuit.

1           30.     The method of claim 29 wherein each of the transistors is a vertical  
2 MOSFET and formation of each transistor includes formation of a source/drain region at  
3 least partially within the semiconductor layer.

1           31.     The method of claim 29 wherein formation of the first transistor includes  
2 formation of a first doped region of a first conductivity type in the semiconductor layer  
3 and formation of the second transistor includes formation of a second doped region of a  
4 second conductivity type in the semiconductor layer.